Physical Design for Nanometer ICs
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Some slides courtesy by Prof. Yao-Wen Chang of NTU EE
Course Contents

- Partitioning
- Floorplanning
- Placement
- Global and detailed routing
- Clock tree synthesis
- Power/Ground network synthesis
Administrative Matters

- **Time:** Wednesdays 9:10am--12:00pm; 92371電機系館
- **Instructor:** Jai-Ming Lin (林家民)
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- **Office:** Room 95305, Chimei Building.
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Books

❖ **Required Text:** Any of the following two books:


❖ **References:** Selected reading materials from recent publications.