Syllabus

Level: undergraduate students (sophomores, juniors)

Credits: 3

Time: Wednesday 8 ~ A (16:10-19:00)

Location: Lecture: EE 92283; Lab: ChiMei 3F SoC Lab

Instructor Information:

Instructor: Prof. 雷曉方 (Sheau-Fang Lei)  Prof. 邱瀝毅 (Lih-yih Chiou)

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Course website:  http://moodle.ncku.edu.tw

Course Description

下一代 IC 在單一晶片上將擁有十億級的電晶體。IC 設計者面對如此複雜系統將面臨前所未有的挑戰。因此，常常利用先進 CAD 工具幫助此複雜系統的開發，藉以減少設計困難度、提高設計生產力。此課程目的在於介紹 IC 設計程序所需之基本知識和工具。在課程設計中，除了教授 IC 設計的基本原理外，也要透過國家晶片設計中心在成大的軟硬體設備，讓同學親自動手設計。使同學在完成此課程後能兼具基本學理及實際設計經驗，並奠定日後繼續進修進階 VLSI/CAD 課程的基礎。課程分為兩部份: IC 數位系統設計 (digital system) 及 IC 電路設計 (circuit)。在修完本課程之後，你會學到

- IC design flow
- Electronic Design Automation (EDA) basics
- Major EDA tools
- Applications in VLSI/CAD fields

且可繼續修下列課程:

- VLSI 系統設計
- 應用導向 VLSI 晶片設計
- 計算機演算法
- VLSI 電路設計
Pre-requisite Courses:
- Microelectronics I, Digital logic, and basic programming skills

Course Materials:

Textbook:
- Lecture notes on course website
- Lab manuals on course website

Reference books:

EDA Tools:
- Hspice (Synopsys), Virtuso & Composer (Cadence), Laker (SpringSoft)
- Verilog XL (Cadence), Design Vision (Synopsys)

Important Date:
- Part I Mini Project Demo: 17:10pm-18:00pm Wednesday, April 20, 2011
- Part II Final exam: 16:10pm-18:00pm Wednesday, June 15, 2011

- There will be no make-up exams (in very special circumstances, written excuse and official proofs are required for make-up exams).
Laboratory Assignments

There will be laboratory work except holiday and examines through out the semester. Due day will be specified in the laboratory manual.

- To get credit for your laboratory assignments, your submissions must be done professionally and seriously. Your official name, course number and laboratory number must be visibly shown in each assignment.
- All submission will be done electronically through the course website before the specified time. If you fail to do so, your assignment is considered OVERDUE and gets reduced credits as specified in class.

Grading Policy

Grading will be based on the following items:

- Participation
- Lab assignments
- Final exam

Course Policy

- Encourage you to discuss assigned problems with peers
- Must complete his/her assignment independently or as specified
- Any person/team who is found to be dishonesty in laboratory assignments, examines/quizzes, the involved person(s) will receive an “0” on the evaluated instrument (exam, lab work, etc.)