**Syllabus**

**Instructor:** Ming-Der Shieh (謝明得)

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**Office hours:** (Tue) 15:00~18:00

**Classes:** 92171, (Wed) 13:10~16:00 (2010)

**Text Book:**


**References:**

7. [http://grouper.ieee.org/groups/1500](http://grouper.ieee.org/groups/1500)
Course Description:
In the course of this semester, you will learn the state-of-the-art digital IP design concepts and techniques including authoring, synthesis, FPGA prototyping, testing, and deliverables, etc. It is hoped that you will have the capability of creating good and valuable IPs and be ready for SoC challenges.

Prerequisite:
Basic VLSI/ASIC Design, Fundamental Logic/Test course, EDA/CAD Design

Outline:
1. Introduction to SoC/IP design
2. IP Authoring
3. Synthesis techniques
4. FPGA Prototyping and Verification
5. IP/SoC Testing
6. IP Deliverables

Grading:
The final grade will be computed on the basis of the following weights.
1. Homework 30%
2. Minterm 30%
3. Term Project and Presentation 40%